1024 x 4-BIT STATIC CMOS RAM

DESCRIPTION

The μPD444 is a high-speed, low power silicon gate CMOS 4096 bit static RAM organized 1024 words by 4 bits. It uses DC stable (static) circuitry throughout and therefore requires no clock or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out non-destructively and has the same polarity as the input data. Common input/output pins are provided.

$\overline{CS}$ controls the power down feature. In less than a cycle time after $\overline{CS}$ goes high — deselecting the μPD444 — the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ is high. There is no minimum $\overline{CS}$ high time for device operation, although it will determine the length of time in the power down mode. When $\overline{CS}$ goes low, selecting the μPD444, the μPD444 automatically powers up.

The μPD444 is placed in an 18-pin plastic package for the highest possible density. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The μPD444 is pin-compatible with the μPD2114L NMOS Static RAM.

Data retention is guaranteed to 2 volts on all parts. These devices are ideally suited for low power applications where battery operation or battery backup for non-volatility is required.

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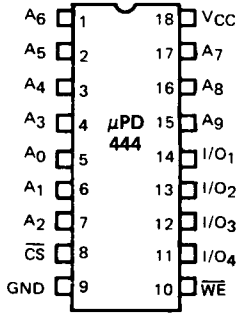
FEATURES

- Low Power Standby — 1 μA Typ.
- Low Power Operation
- Data Retention — 2.0V Min.
- Capability of Battery Backup Operation
- Fast Access Time — 200-450 ns
- Identical Cycle and Access Times
- Single +5V Supply
- No Clock or Timing Strobe Required
- Completely Static Memory
- Automatic Power-Down
- Directly TTL compatible: All Inputs and Outputs
- Common Data Input and Output using Three-State Outputs
- Available in a Standard 18-Pin Plastic Package
- For Operation at +3V Power Supply, Contact the NEC Sales Office.

PIN CONFIGURATION



Rev/2

PIN NAMES

A_0-A_9	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

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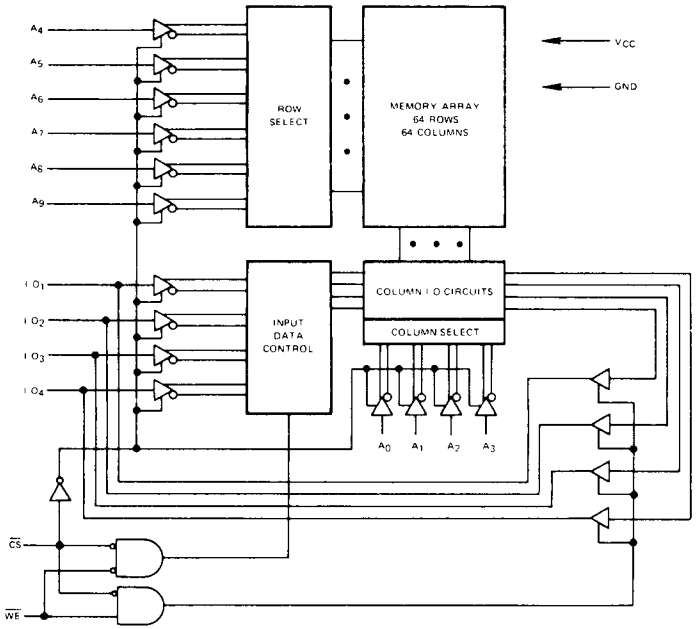
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
All Input and Output Voltages	-0.3 to V_{CC} +0.3 Volts ①
Supply Voltage	+8.0 Volts

Note: ① With Respect to Ground

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = -40°C to +85°C; V_{CC} = +5V ± 10% unless otherwise noted.

PARAMETER	SYMBOL	LIMITS 444-3 MIN	444-3 TYP	444-3 MAX	444-2 MIN	444-2 TYP	444-2 MAX	444-1 MIN	444-1 TYP	444-1 MAX	444 MIN	444 TYP	444 MAX	UNIT	TEST CONDITIONS
Input Leakage Current	I_{LI}	-1.0		1.0	-1.0		1.0	-1.0		1.0	-1.0		1.0	μA	V_{IN} = GND to V_{CC}
I/O Leakage Current	I_{LO}	-1.0		1.0	-1.0		1.0	-1.0		1.0	-1.0		1.0	μA	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}
Operating Supply Current	I_{CCA1}		19	35		15	35		12	35		9	35	mA	$\overline{CS}$ = V_{IL}, V_{IN} = V_{CC}, Outputs Open
Operating Supply Current	I_{CCA2}		23	70		19	40		15	40		12	40	mA	$\overline{CS}$ = V_{IL}, V_{IN} = 2.4V, Outputs Open
Average Operating Supply Current	I_{CCA3}		10	20		9	20		8	20		7	20	mA	V_{IN} = GND or V_{CC}, Outputs Open f = 1 MHz, Duty 50%
Standby Supply Current	I_{CCS}		1	5		1	5		1	5		1	50	μA	$\overline{CS}$ = V_{CC}, V_{IN} = GND to V_{CC}
Input Low Voltage	V_{IL}	-0.3		0.8	-0.3		0.8	-0.3		0.8	-0.3		0.8	V	
Input High Voltage	V_{IH}	2.4		V_{CC} + 0.3	2.4		V_{CC} + 0.3	2.4		V_{CC} + 0.3	2.4		V_{CC} + 0.3	V	
Output Low Voltage	V_{OL}			0.4			0.4			0.4			0.4	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4			2.4			2.4			2.4			V	I_{OH} = -1.0 mA

CAPACITANCE

T_a = 25 C, f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input/Output Capacitance	$C_{I/O}$			10	pF	$V_{I/O}$ = 0V
Input Capacitance	C_{IN}			5	pF	V_{IN} = 0V

Note: This parameter is periodically sampled and not 100% tested.

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AC CHARACTERISTICS

T_a = −40°C to +85°C; V_{CC} = +5V ± 10% unless otherwise noted.

PARAMETER	SYMBOL	LIMITS 444-3 MIN	444-3 MAX	444-2 MIN	444-2 MAX	444-1 MIN	444-1 MAX	444 MIN	444 MAX	UNIT	TEST CONDITIONS
READ CYCLE											
Read Cycle	t_{RC}	200		250		300		450		ns	Input Pulse Levels: +0.8 to +2.4 Volts
Address Access Time	t_{AA}		200		250		300		450	ns	Input Rise and Fall Times: 10 ns
Chip Select Access Time ①	t_{ACS1}		200		250		300		450	ns	Input and Output Timing Levels: 1.5 Volt
Chip Select Access Time ②	t_{ACS2}		250		300		350		500	ns	Output Load: 1 TTL Gate and C_L = 100 pF
Output Hold from Address Change	t_{OH}	50		50		50		50		ns	
Chip Selection to Output in Low Z	t_{LZ}	20		20		20		20		ns	
Chip Deselection to Output in High Z	t_{HZ}		60		70		80		100	ns	
WRITE CYCLE											
Write Cycle Time	t_{WC}	200		250		300		450		ns	Input Pulse Levels: +0.8 to +2.4 Volts
Chip Selection to End of Write	t_{CW}	180		230		250		350		ns	Input Rise and Fall Times: 10 ns
Address Valid to End of Write	t_{AW}	180		230		250		350		ns	Input and Output Timing Levels: 1.5 Volt
Address Setup Time	t_{AS}	0		0		0		0		ns	Output Load: 1 TTL Gate and C_L = 100 pF
Write Pulse Width	t_{WP}	180		210		230		300		ns	
Write Recovery Time	t_{WR}	0		0		0		0		ns	
Data Valid to End of Write	t_{DW}	120		140		150		200		ns	
Data Hold Time	t_{DH}	0		0		0		0		ns	
Write Enabled to Output in High Z	t_{WZ}		60		70		80		100	ns	
Output Active from End of Write	t_{OW}	0		0		0		0		ns	

Notes: ① Chip deselected for greater than 100 ns prior to selection.

② Chip deselected for a finite time that is less than 100 ns prior to selection. (If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle No. 1.)

LOW V_{CC} DATA RETENTION CHARACTERISTICS

T_a = −40°C to +85°C

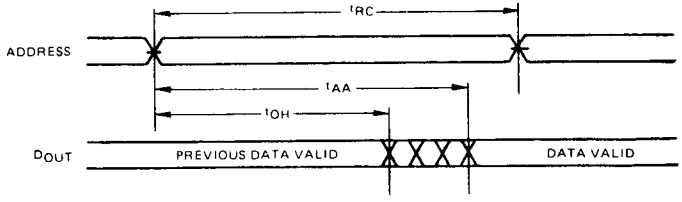
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Data Retention Supply Voltage	V_{CCDR}	2.0			V	$\overline{CS}$ = V_{CC}, V_{IN} = V_{CC} to GND
Data Retention Supply Current	I_{CCDR}		0.01	②	μA	V_{CC} = 3V, $\overline{CS}$ = V_{CC} V_{IN} = V_{CC} to GND
Chip Deselect to Data Retention Time	t_{CDR}	0			ns	
Operation Recovery Time	t_R	t_{RC} ①			ns	

Notes: ① t_{RC} = Read Cycle Time

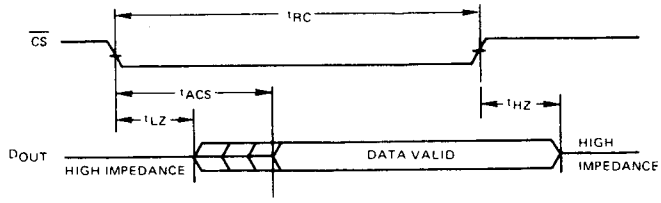
② 444-1, -2, -3: Value is 2 μA
444 Value is 10 μA

TIMING WAVEFORMS

READ CYCLE ① ②



READ CYCLE ① ③



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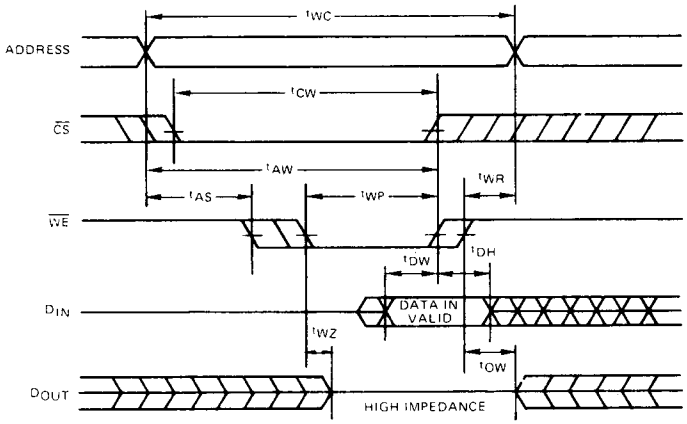
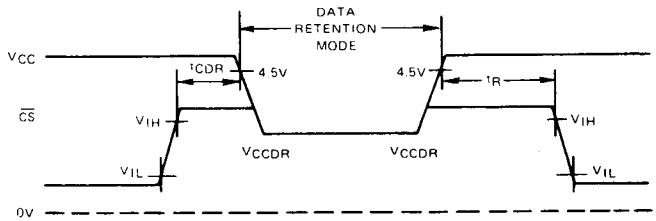
WRITE CYCLE ④ ⑤ ⑥

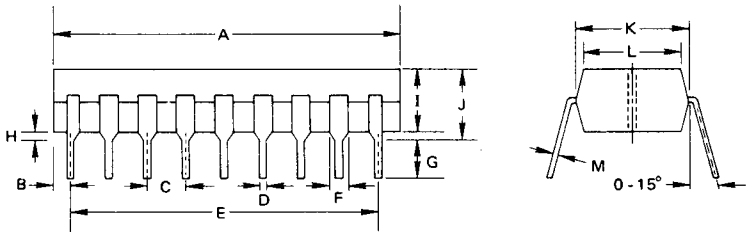


Notes: ① $\overline{WE}$ is high for Read Cycles.
② Device is continuously selected, $\overline{CS}$ = V_{IL}.
③ Address valid prior to or coincident with $\overline{CS}$ transition low.
④ If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition, the output buffers remain in a high impedance state.
⑤ $\overline{WE}$ must be high during all address transitions.
⑥ t_{WP} is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.

LOW V_{CC} DATA RETENTION



PACKAGE OUTLINE
μPD444C



Plastic

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.05
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

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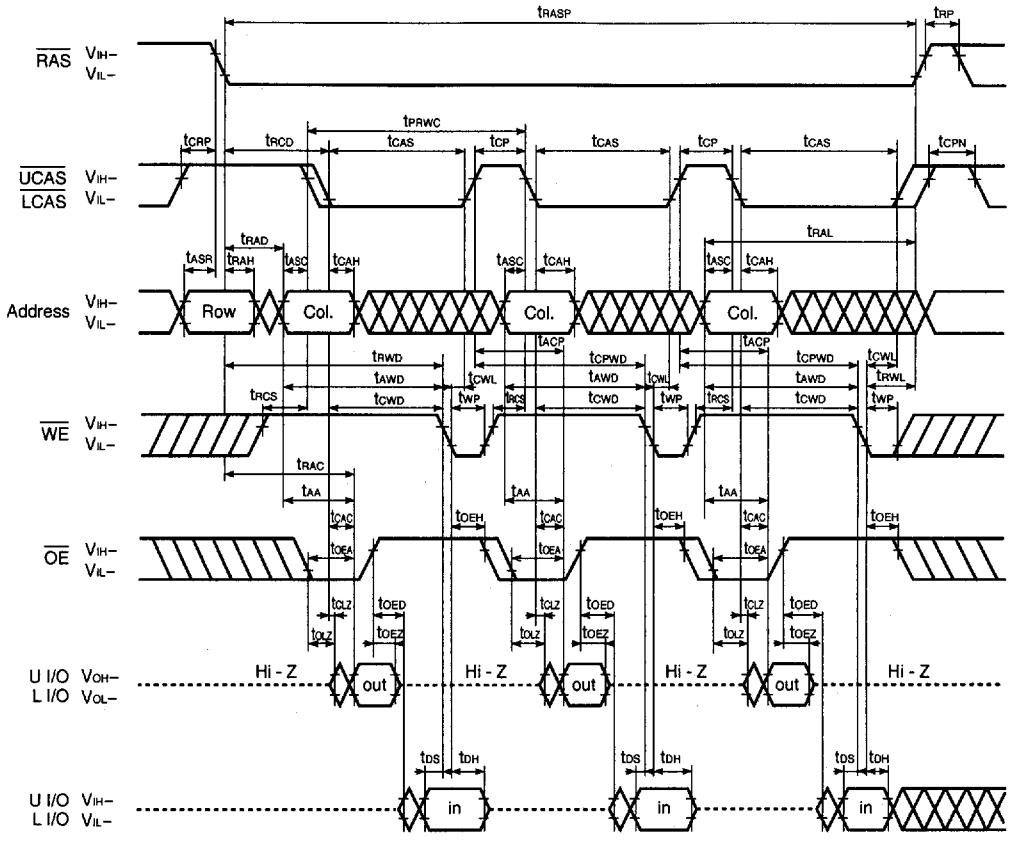
Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

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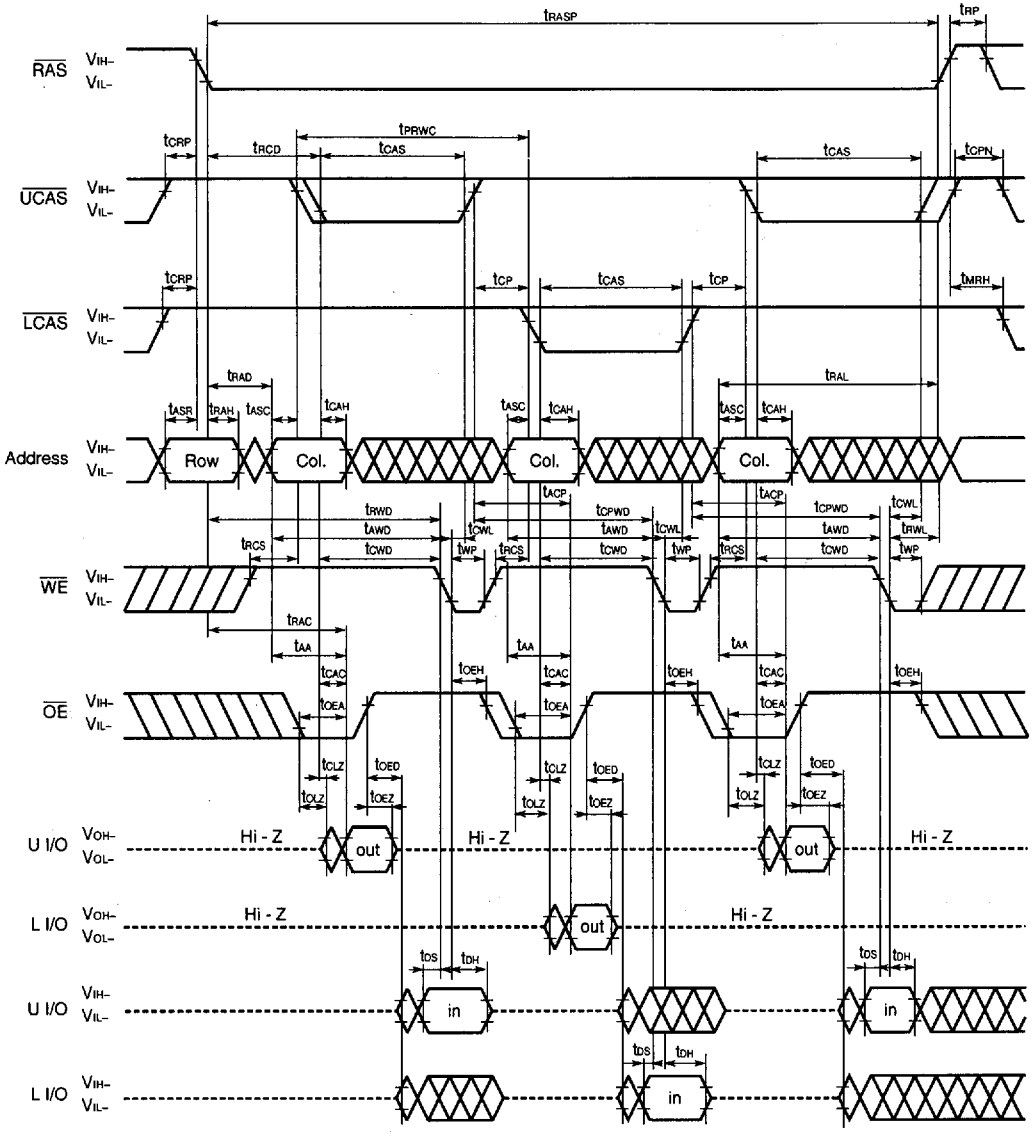
Fast Page Mode Byte Read Modify Write Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

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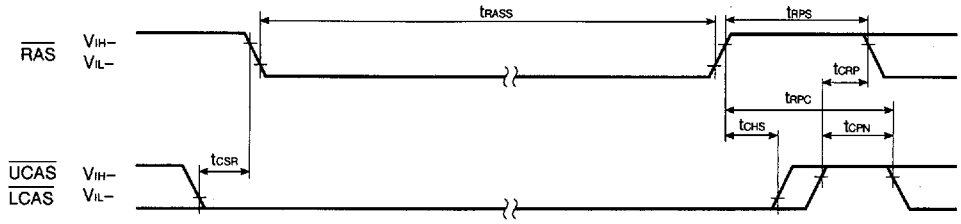
$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S18160)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

μPD42S18160: 1,024 times within a 16 ms interval

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

μPD42S18160: 1,024 times within a 16 ms interval

(3) If $t_{RASS\ (MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles as follows should be met.

μPD42S18160: 1,024 times within a 128 ms interval

For details, please refer to **How to use DRAM** User's Manual.

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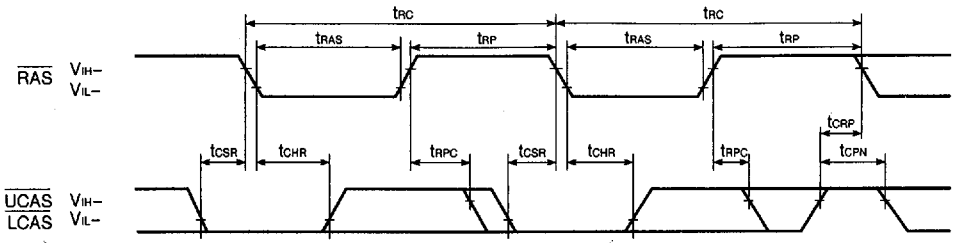
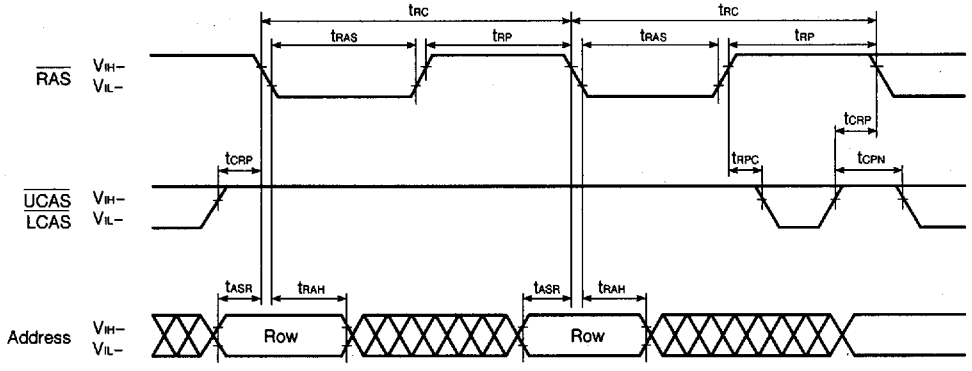
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle



Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

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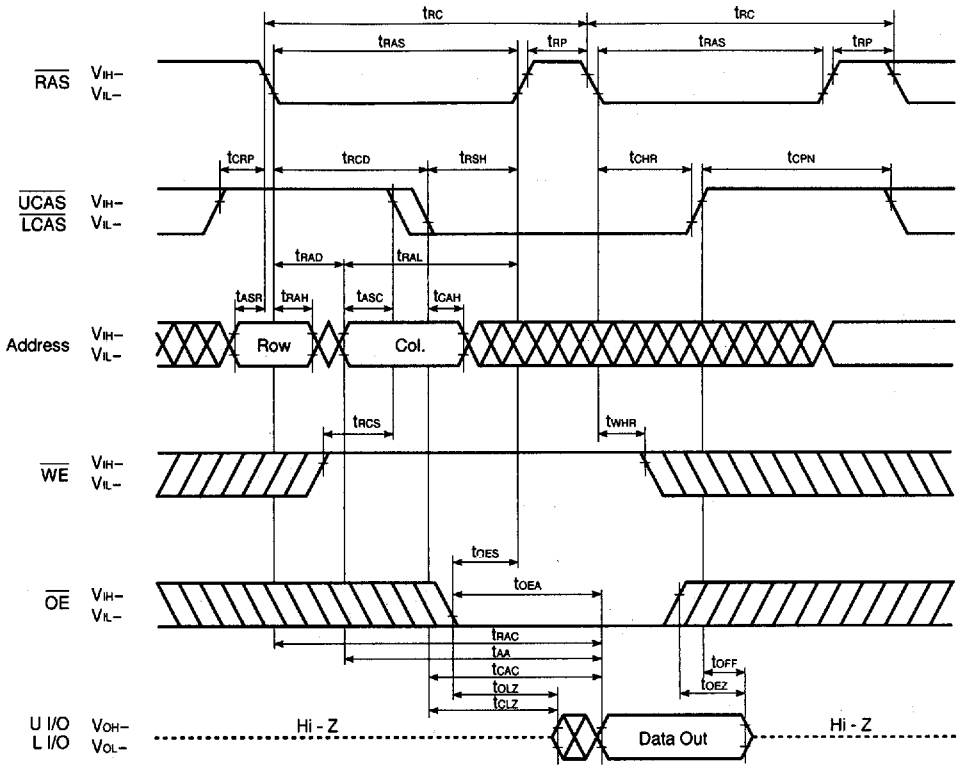
Hidden Refresh Cycle (Read)



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